

Listing of the Claims:

The following is a complete listing of all the claims in the application, with an indication of the status of each:

- 1 1 (Original). A simulation method for simulating a system having a
2 plurality of circuit modules using software, comprising the steps of:
3 using an object oriented language;
4 preparing a plurality of circuit base classes, which describe base
5 circuit modules as classes, as a library;
6 describing the circuit modules to be simulated as classes by
7 inheriting the circuit base classes prepared as the library; and
8 describing the system to be simulated by combining the circuit
9 modules described as the classes.

- 1 2 (Original). A simulation method according to claim 1, further comprising
2 the step of describing the system as a class by inheriting the circuit base
3 classes prepared in the library.

- 1 3 (Currently Amended). A simulation method according to claim 1, further
2 comprising the step of preparing a component class having the properties
3 of a circuit which contains a circuit operating asynchronously with a clock
4 signal, and a synchronous module class, having the properties of a circuit
5 operating synchronously with the clock signal in the library, which is
6 derived from said component class.

- 1 4 (Original). A simulation method according to claim 3, further comprising
2 the step of preparing a bus class having the properties of a bus, a bus
3 master class having the properties of a bus master, and a bus slave class
4 having the properties of a bus slave, as the circuit base class described as a
5 class derived from the synchronous module class, in the library.

1 5 (Original). A simulation method according to claim 4, further comprising
2 the step of preparing a bus master interface class, whose base classes are
3 the synchronous module class, and which has the properties of a bus
4 master interface, and a bus slave interface class having the properties of a
5 bus slave interface, as the circuit base class in the library.

1 6 (Original). A simulation method according to claim 3, further comprising
2 the step of preparing a central processing unit class, whose base class is the
3 synchronous module class, and which has the properties of a central
4 processing unit, as the circuit base class in the library.

1 7 (Original). A simulation method according to claim 3, further comprising
2 the step of preparing a hierarchy class, whose base class is the synchronous
3 module class, and which has the properties of a hierarchy of a circuit
4 containing the bus, as the circuit base class in the library.

1 8 (Original). A simulation method according to claim 4, further comprising
2 the step of preparing a memory class, whose base class is the bus slave
3 class, and which has the properties of a memory, as the circuit base class in
4 the library.

1 9. (Previously Presented). A simulating apparatus, using a computer, for
2 simulating a system having a plurality of circuit modules, said simulation
3 apparatus comprising:
4 storage means storing a plurality of circuit base classes, which
5 describe base circuit modules as classes, as a library;
6 means accessing the storage means and describing the circuit
7 modules to be simulated as classes by inheriting the circuit base classes
8 stored in the library; and

9 means combining the circuit modules described as classes to
10 describe the system to be simulated.

1 10 (Previously Presented). A computer-readable storage medium for
2 storing a computer program for executing a simulation method for
3 simulating a system having a plurality of circuit modules, the computer
4 program comprising the steps of:
5 using an object oriented language;
6 preparing a plurality of circuit base classes, which describe base
7 circuit modules as classes, as a library;
8 describing the circuit modules to be simulated as classes by
9 inheriting the circuit base classes prepared as a library; and
10 describing the system to be simulated by combining the circuit
11 modules described as classes.

1 11 (New). A simulating apparatus according to claim 9, wherein the means
2 combining the circuit modules describes the system to be simulated as a
3 class by inheriting the circuit base classes prepared in the library.

1 12 (New). A simulating apparatus according to claim 9, wherein the
2 storage means stores a component class having the properties of a circuit
3 which contains a circuit operating asynchronously with a clock signal, and
4 a synchronous module class, having the properties of a circuit operating
5 synchronously with the clock signal in the library, which is derived from
6 said component class.

1 13 (New). A simulating apparatus according to claim 12, wherein the
2 storage means stores a bus class having the properties of a bus, a bus
3 master class having the properties of a bus master, and a bus slave class
4 having the properties of a bus slave, as the circuit base class described as a

5 class derived from the synchronous module class, in the library.

1 14 (New). A simulating apparatus according to claim 13, where in the
2 storage means stores a bus master interface class, whose base classes are
3 the synchronous module class, and which has the properties of a bus
4 master interface, and a bus slave interface class having the properties of a
5 bus slave interface, as the circuit base class in the library.

1 15 (New). A simulating apparatus according to claim 12, wherein the
2 storage means stores a central processing unit class, whose base class is the
3 synchronous module class, and which has the properties of a central
4 processing unit, as the circuit base class in the library.

1 16 (New). A simulating apparatus according to claim 12, wherein the
2 storage means stores a hierarchy class, whose base class is the synchronous
3 module class, and which has the properties of a hierarchy of a circuit
4 containing the bus, as the circuit base class in the library.

1 17 (New). A simulating apparatus according to claim 13, wherein the
2 storage means stores a memory class, whose base class is the bus slave
3 class, and which has the properties of a memory, as the circuit base class in
4 the library.

1 18 (New). A computer-readable storage medium according to claim 10,
2 wherein the computer program further comprises the step of describing the
3 system as a class by inheriting the circuit base classes prepared in the
4 library.

1 19 (New). A computer-readable storage medium according to claim 10,
2 wherein the computer program further comprises the step of preparing a

3 component class having the properties of a circuit which contains a circuit
4 operating asynchronously with a clock signal, and a synchronous module
5 class, having the properties of a circuit operating synchronously with the
6 clock signal in the library, which is derived from said component class.

1 20 (New). A computer-readable storage medium according to claim 19,
2 wherein the computer program further comprises the step of preparing a
3 bus class having the properties of a bus, a bus master class having the
4 properties of a bus master, and a bus slave class having the properties of a
5 bus slave, as the circuit base class described as a class derived from the
6 synchronous module class, in the library.

1 21 (New). A computer-readable storage medium according to claim 20,
2 wherein the computer program further comprises the step of preparing a
3 bus master interface class, whose base classes are the synchronous module
4 class, and which has the properties of a bus master interface, and a bus
5 slave interface class having the properties of a bus slave interface, as the
6 circuit base class in the library.

1 22 (New). A computer-readable storage medium according to claim 19,
2 wherein the computer program further comprises the step of preparing a
3 central processing unit class, whose base class is the synchronous module
4 class, and which has the properties of a central processing unit, as the
5 circuit base class in the library.

1 23 (New). A computer-readable storage medium according to claim 19,
2 wherein the computer program further comprises the step of preparing a
3 hierarchy class, whose base class is the synchronous module class, and
4 which has the properties of a hierarchy of a circuit containing the bus, as
5 the circuit base class in the library.

- 1 24 (New). A computer-readable storage medium according to claim 20,
- 2 wherein the computer program further comprises the step of preparing a
- 3 memory class, whose base class is the bus slave class, and which has the
- 4 properties of a memory, as the circuit base class in the library.